Synchronous Operation of Intersil Rad Hard SOS 64K Asynchronous SRAMs

Application Note | June 1992 | AN9011

The Intersil SOS 64K SRAMs provide excellent single event and total dose hardness, and fast access and cycle times. The HS-65643RH and HS-65647RH were designed as standard pinout asysnchronous circuits; they can, however, be used in systems that require their speed and radiation resistance, but have been designed for synchronous memories. The addition of two HCS373 or HCTS373 to latch the address location on the falling edge of the chip enable signal will make the HS-65643RH and HS-65647RH appear as synchronous memories to the system. The only difference in signal wiring need to use the asynchronous circuits it to route the address lines through the 373's and connect the $\overline{E}$ or $\overline{E1}$ signal to the 373's $\overline{LE}$ pin as shown in Figure 1.

The HCS373 and HCTS373 are both fabricated with SOS technology; each circuit is available hardened to 200K RADs or 1M RADs, and has excellent single event immunity. The addition of the latches will delay the address inputs to the SRAMs by a maximum of 39ns (over temperature, VDD, and 1M RAD total dose), so system timing should be analyzed accordingly. Even with the additional delay of the latches, address access time is a maximum of 89ns (for a 50ns SRAM access time).

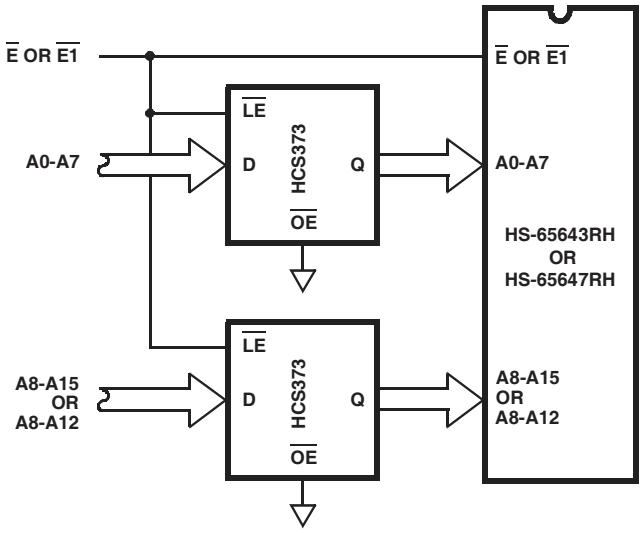
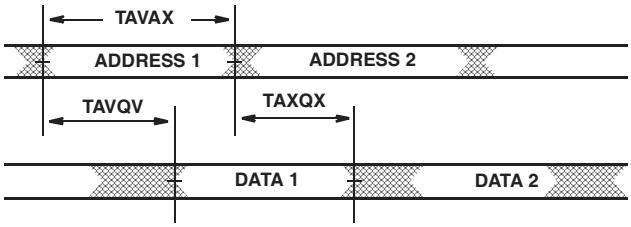


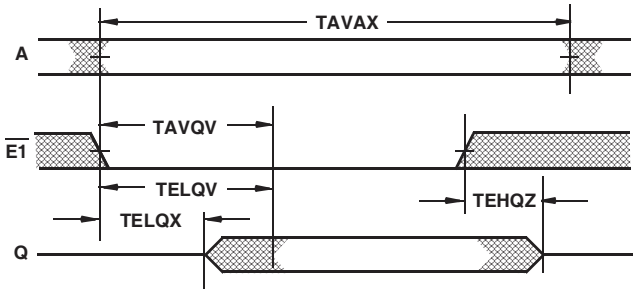
FIGURE 1.

HS-65643RH, HS-65647RH Asynchronous Read Cycles

READ CYCLE I: $\overline{W}$ HIGH; $\overline{G}$, $\overline{E1}$ LOW

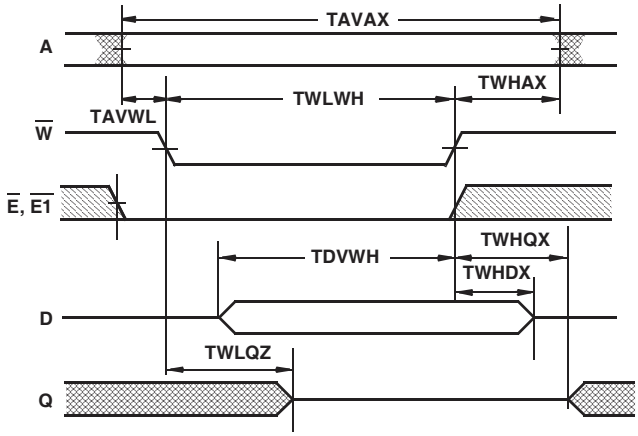


READ CYCLE II: $\overline{W}$ HIGH

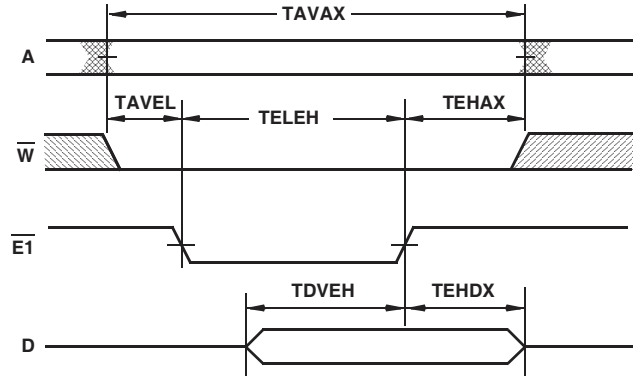


HS-65643RH, HS-6547RH Asynchronous Write Cycles

WRITE CYCLE I: LATE WRITE

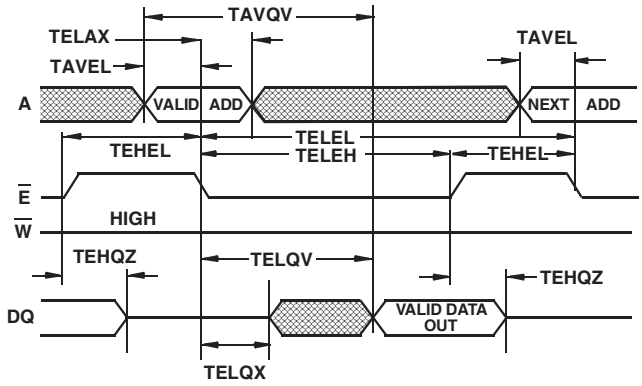


WRITE CYCLE II: EARLY WRITE - CONTROLLED BY $\overline{E}$, $\overline{E1}$



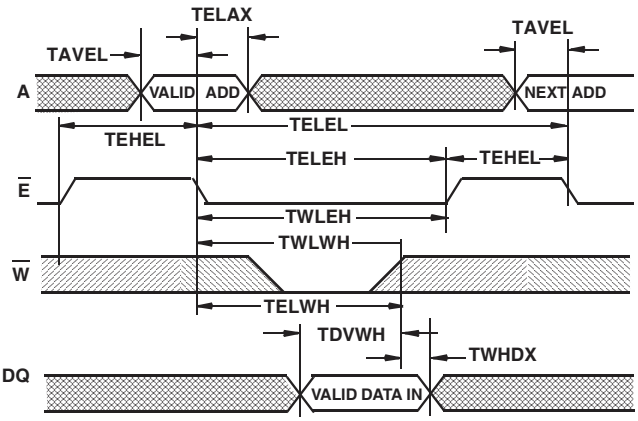
HS-65643RH, HS-65647RH Synchronous Operation

READ CYCLE



The address information is latched in the HSC373's on the falling edge of $\overline{E}$ or $\overline{E1}$; minimum address setup and hold time requirements at the SRAM must be met. After the required hold time, the addresses may change state without affecting device operation. $\overline{W}$ must remain high throughout the read cycle. After the data has been read, $\overline{E}$ or $\overline{E1}$ may return high. This will force the output buffers into a high impedance mode after TEHQZ elapses.

WRITE CYCLE



The write cycle is initiated on the falling edge of $\overline{E}$ or $\overline{E1}$ which latches the address information in the HCS373's. TDVWH and TWHDX at the SRAM inputs must be met for proper device operation. If $\overline{E}$ or $\overline{E1}$ rises before $\overline{W}$ rises, reference data setup and hold times to the $\overline{E}$ or $\overline{E1}$ rising edge. The write operation is terminated by the first rising edge of $\overline{W}$, $\overline{E}$, or $\overline{E1}$. After the minimum $\overline{E}$ high time (TEHEL), the next cycle may begin. If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may be held low until all desired locations have been written. In this case, data setup and hold times must be referenced to the rising edge of $\overline{E}$ or $\overline{E1}$.

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